REMARKS

The Examiner has rejected Claims 1-12, 18-21, 24-28, and 30 under 35 U.S.C. 103(a) as being unpatentable over Rivard (U.S. Patent No. 5,987,567), in view of Wang (U.S. Patent No. 5,831,640), in view of Ando (U.S. Patent No. 5,497,496), and further in view of Ireton (U.S. Patent No. 5,826,089). Further, the Examiner has rejected Claims 13-17, 22, 23, and 29 under 35 U.S.C. 103(a) as being unpatentable over Rivard, in view of Wang, in view of Ando, in view of Ireton, and further in view of Applicant Admitted Prior Art (AAPA). Applicant respectfully disagrees with such rejections, especially in view of the amendments made hereinabove to the independent claims.

Specifically, applicant has amended the independent claims to at least substantially include the following:

> "wherein a particular texture ID is used to refer to the instruction set that is stored as an instruction texture and the particular texture ID is configured to use point sampling so the instruction set is passed without any processing" (see this or similar, but not necessarily identical language in the independent claims).

Applicant respectfully asserts that Ando teaches that "FIG. 4 shows a general structure of a conventional superscalar processor," where "[i]n the figure, a plurality of instructions to be processed are stored in an instruction memory 1," "[a]n instruction fetch circuit 2 reads out a plurality of instructions (for example, four instructions) from instruction memory 1 at the same time and fetches the same," and "[a]n instruction decoder 3 decodes the plurality of instructions fetched by instruction fetch circuit 2, selects instructions which can be processed in a parallel manner and supplies the same to processing units 4 to 7" (Col. 1, lines 38-47 – emphasis added).

However, simply teaching that a plurality of instructions to be processed are stored in an instruction memory 1, and that an instruction fetch circuit 2 reads out a plurality of instructions from instruction memory 1, as in Ando, simply fails to even

suggest any sort of an "instruction set that is stored as an instruction texture," much less applicant's claimed technique "wherein a particular texture ID is used to refer to the instruction set that is stored as an instruction texture and the particular texture ID is configured to use point sampling so the instruction set is passed without any processing" (emphasis added), as specifically claimed by applicant.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,*947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

Applicant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art excerpts, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above. Thus, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

Still yet, applicant brings to the Examiner's attention the subject matter of new Claims 31-32 below, which are added for full consideration:

> "wherein a rasterizer module coupled to the texture module sends the instruction request to an address generator, the address generator converts the instruction request into pseudo texture coordinates for the texture module, and the address generator outputs the pseudo texture coordinates such that resulting texel data is interpreted as the instruction set by the texture module" (see Claim 31); and

"wherein the instruction set is received as an instruction texture that contains a shader program instead of color data and is referenced by a texture coordinate, the instruction texture utilizes texture ID 0 to refer to the shader program stored as the instruction texture, and the texture ID 0 is configured to use the point sampling so the instruction texture data that includes the shader program is not modified by a shader module" (see Claim 32).

Again, a notice of allowance or a proper prior art showing of all of applicant's claim limitations, in combination with the remaining claim elements, is respectfully requested.

Thus, all of the independent claims are deemed allowable. Moreover, the remaining dependent claims are further deemed allowable, in view of their dependence on such independent claims.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP064).

Respectfully submitted,
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